



Figure 7-14
Peripheral-signal timing

Table 7-20
Expansion slot signals

Pin	Signal	Description
1	I/O SELECT	Normally high; goes low during $\phi 0$ when the 65C02 addresses location \$CnXX, where n is the connector number. This line can drive 10 LS TTL loads.*
2-17	A0-A15	Three-state address bus. The address becomes valid during $\phi 1$ and remains valid during $\phi 0$. Each address line can drive 5 LS TTL loads.*
18	R/W'	Three-state read/write line. Valid at the same time as the address bus; high during a read cycle, low during a write cycle. It can drive 2 LS TTL loads.*